REMARKS

The Office action of April 27, 2004 has been received and its contents carefully noted.

In amended Figures 16, and 17A-E, a label of "Conventional Art" has been added.

Claims 1-15 are pending in this application. Claims 11-15 have been added without the addition of new matter.

Claims 1-3 stand rejected under 35 U.S.C. § 102(e) as being unpatentable over Kanai et al. ("Kanai") (U.S. Patent No. 6,278,494). Applicant respectfully traverses these rejections, and requests allowance thereof in the pending application for the following reasons.

The Claims are Patentable Over the Cited References

Claims 1-3 are not anticipated by Kanai

Claims 1-3 stand rejected under § 102(e) in view of Kanai. Applicant strongly contends that Kanai fails to disclose the features recited in these claims such as a high-frequency signal extracting circuit for extracting a high-frequency signal of the image by calculation based on a signal of a pixel which is to be corrected (a target pixel), a signal of a pixel shifted from the target pixel by m (m being an integer not smaller than 2) pixels in the right or lower direction, and a signal of a pixel shifted from the target pixel by m pixels in the left or upper direction, and an adder for adding the output of the amplitude restricting circuit or

a signal obtained therefrom, as an edge correction signal, to the signal of the target pixel.

Kanai fails to disclose these recited features. Firstly, Kanai discloses an edge correction circuit that uses signals with one-pixel shifts from the signal of a target pixel rather than the m-pixel shift (integer m not smaller than 2) being recited to generate a high-frequency signal. (see FIGs. 1-2; col. 6, lines 36-44; col. 7, lines 56-60). Specifically, Kania states that "…14, an adder for computing a difference s10 between an input signal s1, and a signal s2 obtained by delaying signal s1 one pixel; and 15, an adder for computing a difference s11 between the signal s2 and a signal s3 obtained by further delaying the signal s2 one pixel…that is, signals s10 and s11 are difference signals between the pixel of interest and those before and after the pixel of interest." (see FIGs. 1-2; col. 6, lines 36-44).

Kanai discloses a signal of the pixel of interest (target pixel) as being signal s2 which is output from the first delay unit and is delay time-shifted one pixel from signal s1 while signal s3, output from the second delay unit, is delay time-shifted one pixel from signal s2. Thereafter, Kanai discloses the input of this signal of the target pixel and two other signals (all within one pixel delay from each other) to generate a high-frequency signal s5 which strongly contrasts from the recited feature of extracting a high-frequency signal using signals of a pixel that are m-pixel shifted from the signal of the target pixel where m is no smaller

than 2). Using signals with only a one-pixel shift as disclosed by Kanai is significantly distinct from using signals with a m-pixel shift (where m is no smaller than 2) as recited.

Secondly, Kanai does not add an output of an amplitude restricting circuit to the signal of the target pixel as recited. As disclosed above by Kanai, the signal of the target pixel in his disclosure is the output signal s2 from the first delay unit carrying a one-pixel shift relative to and in-between signals s1, s3. However, Kanai does not disclose adding this signal of the target pixel (s2) to the output signal from the amplitude restricting circuit (s15), but instead adds a further time-delayed version of the signal of the target pixel (s2d), further delayed by delay unit 3, to the output signal from the amplitude restricting circuit (s15) in contrast to the recited feature. (see FIG. 1; col. 6, lines 66-67; col. 7, lines 1-4). Adding a further time-delayed version of the signal of the target pixel (to the output signal from an amplitude restricting circuit) as disclosed by Kanai is significantly distinct from adding the signal of the target pixel as recited.

Further, regarding Claim 3, the Action appears to confuse the amplitude-restricting signal generator and the amplitude restricting circuit disclosed by Kanai. The amplitude-restricting signal generator disclosed by Kanai is limited to subtractors 14, 15 and absolute value circuits 16, 17 which generate two of the inputs for the minimum value circuit 11 which is consistent with

page 3, subsection b of the Action. Therefore, minimum value circuit 11 starts the beginning of the amplitude restricting circuit disclosed by Kanai which is consistent with page 3, subsection c of the Action. However, the Action thereafter engages in inconsistent logic, in an attempt to reject Claim 3, as multiplier 19 cannot be considered the recited amplitude adjuster of the output signal from amplitude-restricting signal generator since the amplitude-restricting signal generator comprises the subtractors 14, 15 and absolute value circuits 16, 17 as admitted by page 3, subsection b of the Action. The multiplier 19 is a part of the amplitude restricting circuit, rather than the amplitude-restricting signal generator, as clearly illustrated in FIG. 1 of Kanai and consistent with the page 3, subsection c of the Action. Multiplier 19 cannot jump from being part of the amplitude restricting circuit (coming after minimum value circuit 11) of Kanai to being part of the amplitude-restricting signal generator which is limited to subtractors 14, 15 and absolute value circuits 16, 17 as illustrated in FIG. 1, and therefore cannot be considered as an amplitude adjuster of the amplitude-restricting signal generator as recited.

Kanai fails to disclose the above-mentioned recited features of these claims making the claimed invention patentably distinct and non-obvious from the disclosed prior art.

Conclusion

In view of the amendments and remarks submitted above, it is respectfully submitted that all of the remaining claims are allowable and a Notice of Allowance is earnestly solicited.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayments to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

The Examiner is invited to contact the undersigned at (703) 205-8000 to discuss the application.

Respectfully submitted,

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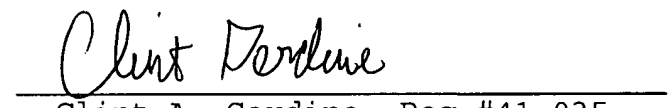
by 

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Attachment: Replacement Drawings (2)
Letter Requesting Initialed PTO 1449 Form